



Network-on-Chip: The Next Generation of System-on-Chip Integration

By Santanu Kundu, Santanu Chattopadhyay

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Addresses the Challenges Associated with System-on-Chip Integration

Network-on-Chip: The Next Generation of System-on-Chip Integration examines the current issues restricting chip-on-chip communication efficiency, and explores Network-on-chip (NoC), a promising alternative that equips designers with the capability to produce a scalable, reusable, and high-performance communication backbone by allowing for the integration of a large number of cores on a single system-on-chip (SoC). This book provides a basic overview of topics associated with NoC-based design: communication infrastructure design, communication methodology, evaluation framework, and mapping of applications onto NoC. It details the design and evaluation of different proposed NoC structures, low-power techniques, signal integrity and reliability issues, application mapping, testing, and future trends.

Utilizing examples of chips that have been implemented in industry and academia, this text presents the full architectural design of components verified through implementation in industrial CAD tools. It describes NoC research and developments, incorporates theoretical proofs strengthening the analysis procedures, and includes algorithms used in NoC design and synthesis. In addition, it considers other upcoming NoC issues, such as low-power NoC design, signal integrity issues, NoC testing, reconfiguration, synthesis, and 3-D NoC design.

This text comprises 12 chapters and covers:

- The evolution of NoC from SoC?its research and developmental challenges
- NoC protocols, elaborating flow control, available network topologies, routing

mechanisms, fault tolerance, quality-of-service support, and the design of network interfaces

- The router design strategies followed in NoCs
- The evaluation mechanism of NoC architectures
- The application mapping strategies followed in NoCs
- Low-power design techniques specifically followed in NoCs
- The signal integrity and reliability issues of NoC
- The details of NoC testing strategies reported so far
- The problem of synthesizing application-specific NoCs
- Reconfigurable NoC design issues
- Direction of future research and development in the field of NoC

Network-on-Chip: The Next Generation of System-on-Chip Integration covers the basic topics, technology, and future trends relevant to NoC-based design, and can be used by engineers, students, and researchers and other industry professionals interested in computer architecture, embedded systems, and parallel/distributed systems.

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Editorial Review

Review

"What makes this book special as compared to the current literature in the field is that it provides a complete picture of NoC architectures. In fact, current books in the context of NoCs are usually specific and presuppose a basic knowledge of NoC architectures. Conversely, this book provides a complete guide for both unskilled readers and researchers working in the area, to acquire not only the basic concepts but also the advanced techniques for improving power, cost and performance metrics of the on-chip communication system."

?Maurizio Palesi, Kore University, Italy

About the Author

Santanu Kundu received his BTech in instrumentation engineering from Vidyasagar University, Medinipur, West Bengal, India, in 2002. He received his MTech in instrumentation and electronics engineering from Jadavpur University, Kolkata, West Bengal, India, in 2006. Immediately after that he joined the electronics and electrical communication engineering department at the Indian Institute of Technology, Kharagpur, West Bengal, India. He received his PhD in 2011. His research interests include network-on-chip architecture design in 2D and 3D environments, performance and cost evaluation, signal integrity in nanometer regime, fault-tolerant schemes, and power–performance–reliability trade-off. He is currently a system-on-chip (SoC) design engineer at LSI India R&D Pvt. Ltd., Bangalore, Karnataka, India.

Santanu Chattopadhyay received his BE in computer science and technology from Calcutta University (BE College), Kolkata, West Bengal, in 1990. In 1992 and 1996, he received his MTech in computer and information technology and PhD in computer science and engineering, respectively, both from the Indian Institute of Technology (IIT), Kharagpur, West Bengal, India. He is currently a professor in the electronics and electrical communication engineering department at the IIT, Kharagpur. He has contributed to more than 100 publications in refereed international journals and conferences. He has also coauthored and written several textbooks, and is a member of the editorial board of the journal *IET Circuits, Devices and Systems*.

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