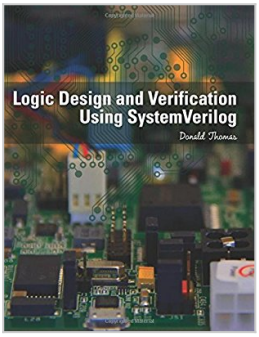

Logic Design and Verification Using SystemVerilog

By Donald Thomas

Logic Design and Verification Using SystemVerilog By Donald Thomas

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SystemVerilog is a Hardware Description Language that enables designers to work at the higher levels of logic design abstractions that match the increased complexity of current day integrated circuit and field-programmable gate array (FPGA) designs. The majority of the book assumes a basic background in logic design and software programming concepts. It is directed at: • students currently in an introductory logic design course that also teaches SystemVerilog, • designers who want to update their skills from Verilog or VHDL, and • students in VLSI design and advanced logic design courses that include verification as well as design topics. The book starts with a tutorial introduction on hardware description languages and simulation. It proceeds to the register-transfer design topics of combinational and finite state machine (FSM) design — these mirror the topics of introductory logic design courses. The book covers the design of FSM-datapath designs and their interfaces, including SystemVerilog interfaces. Then it covers the more advanced topics of writing testbenches including using assertions and functional coverage. A comprehensive index provides easy access to the book’s topics. The goal of the book is to introduce the broad spectrum of features in the language in a way that complements introductory and advanced logic design and verification courses, and then provides a basis for further learning.

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Editorial Review

About the Author
Donald Thomas is Professor of Electrical and Computer Engineering at Carnegie Mellon University, where he has taught courses Logic Design and Verification, and Embedded Systems. His former book, The Verilog Hardware Description Language, was co-authored with Verilog inventor Phil Moorby and was widely used in industry and universities. His research topics include high-level synthesis, register-transfer level simulation and languages, hardware-software co-design, integrated circuit lifetime reliability, and hardware-based machine leaning.

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